

Abstract of the Invention

TIMING CLOSURE METHODOLOGY

An automated method for designing an integrated circuit layout using a computer based upon an electronic circuit description and based upon cells which are selected from a cell library, each of the cells having an associated area, comprising the steps of: (a) placing each of the cells in the integrated circuit layout so that the cells can be coupled together by wires to form a circuit path having an associated predetermined delay constraint wherein the cells are coupled together based upon the electronic circuit description input to the computer; (b) connecting the cells together with the wires to form the circuit path; and (c) adjusting an area of at least one of the cells to satisfy the associated predetermined delay constraint of the circuit path.